ABSTRACT OF THE DISCLOSURE

An integrated circuit with both P-channel transistors (823) and N-channel transistors (821) with different spacer insulating region widths. In one example, the outer sidewall spacer (321) of the N-channel transistors is removed while the P-channel regions (115) are masked such that the spacer insulating region widths of the N-channel transistors is less than the spacer insulating region widths of the P-channel transistors. Also, the drain/source silicide regions (805) of the N-channel transistors are located closer to the gates (117) of those transistors than the P-channel source/drain silicide regions (809) are located to the gates (119) of those transistors. Providing the P-channel transistors with greater spacer insulating widths and greater distances between the source/drain silicide regions and gates may increase the relative compressive stress of the channel region of the P-channel transistors relative the stress of the channel region of the N-channel transistors, thereby increasing the performance of the P-channel transistors.